Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Original) A semiconductor device comprising:

a borderless logic array; area I/Os; and wherein said logic array comprises a repeating core, and wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least one metal layer that is the same for all I/O configurations.

2. (Cancelled)

3. (Original) A semiconductor wafer comprising:

a borderless logic array, wherein said borderless logic array comprises a repeating module containing logic cells and I/O cells and a redistribution layer for redistributing at least some of said I/O cells' connections to pads used in packaging.

4. (Original) A semiconductor wafer according to claim 3, wherein said I/O cells are arranged in spaced parallel lines.

5. (Original) A semiconductor wafer according to claim 4, wherein spaced parallel lines are spaced at least 0.2 mm apart but less than 3 mm apart.

6. (Original) A semiconductor wafer according to claim 3, wherein said repeating module comprises at least two metal layers.

7. (Original) A semiconductor wafer according to claim 6, wherein at least one of said metal

layers comprises a repeating pattern.

8. (Original) A semiconductor wafer according to claim 6, wherein each of said metal layers comprises a repeating pattern.

9. (Original) A semiconductor wafer according to claim 6, wherein additional custom layers are arranged to form a specific die size on said semiconductor wafer.

10. (Original) A semiconductor wafer according to claim 6, wherein additional custom layers are arranged to form at least two different die sizes on said semiconductor wafer.

11. (Previously Presented) A semiconductor device comprising repeating I/O cells, and wherein said repeating I/O cells comprise configurable I/O cells that are customized to different functions by using only custom via layers.

12. (Original) A semiconductor device according to claim 11, further comprising repeating logic cells, and wherein said semiconductor device is customized by using only custom via layers.

13. (Currently Amended) A semiconductor device according to claim 11, wherein each of said configurable I/O cells comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein said custom via layers are used to complete at least one of said possible connections to configure said configurable I/O cells.

14. (Currently Amended) A semiconductor device according to claim 1, wherein said configurable I/O comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein at least one custom via layer is used to complete at least one of said possible connections to configure said configurable I/O.

15. (Currently Amended) A semiconductor wafer according to claim 3, wherein at least one of said ~~of said~~ I/O cells comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein at least one custom via layer is used to complete at least one of said possible connections to configure at least one of said I/O cells.

16. (Previously Presented) A semiconductor device comprising:

a borderless logic array; area I/Os; and wherein said logic array comprises a repeating core and a redistribution layer for redistributing at least some of said area I/O connections to pads used in packaging.

17. (Previously Presented) A semiconductor device comprising:

a borderless logic array; area I/Os; and wherein at least one of said area I/Os is a configurable I/O, and a redistribution layer for redistributing at least some of said area I/O connections to pads used in packaging.

18. (Previously Presented) A semiconductor device comprising:

a borderless logic array; area I/Os; and wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least one metal layer that is the same for all I/O configurations.

19. (New) A semiconductor wafer according to claim 18, wherein said configurable I/O further comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein a custom via layer is used to complete at least one of said possible connections to configure said configurable I/O.